ADAPTIVE CLOCKING MECHANISM FOR DIGITAL VIDEO DECODER

RELATED APPLICATIONS

The invention is related to US Provisional Application 60/104,250, filed on October 14, 1998, entitled ADAPTIVE CLOCKING MECHANISM FOR DIGITAL TELEVISION, the subject matter thereof being fully incorporated by reference herein.

5 The invention is also related to U.S. Patent Application S/N _____, filed concurrently herewith, entitled ADAPTIVE SYNCHRONIZATION MECHANISM FOR DIGITAL VIDEO DECODER, which is assigned to the same assignee and incorporated by reference herein.

FIELD OF THE INVENTION

10 The invention relates generally to video decoders. More specifically, the invention relates to modifying the clock mechanism of a digital video decoder to allow for synchronization of decoded and encoded standard definition (SD) and high definition (HD) video signals that may have multiple formats and/or frame rates.

BACKGROUND OF THE INVENTION

15 With ever increasing demand for video throughput and a relatively finite transmission infrastructure, compression of video signal information to be transmitted has become essential. Fortunately, the coincident vast increase in digital processing capability has rendered practical the digitization of such video signal information followed by application of various compression algorithms to the digitized data. In 20 the operation of that compression process, the digitized video signal information is operated on by an encoder at the transmission site, which carries out the desired

For the clock-recovery step of the two step decoder synchronization process described in the Background section, an established method of recovering the base clock with respect to MPEG-2 video signals and systems is set forth in Annex D of the ISO/IEC 13818-1 standard (specifically, Section D.0.3 *System Time Clock*

5 *Recovery in the Decoder*). It will be understood that, although this is currently the accepted standard method for decoder timing synchronization with the base clock of MPEG-2 signals (such as used in the transmission of digital television in the U.S.), reference to this method is merely for illustrative purposes, and the subject invention is not limited to such method or to digital television systems.

10 The operation of the ISO/IEC 13818-1 standard clock recovery system is depicted schematically in Figure 1. As will be seen from the figure, either the system clock reference (SCR) or the program clock reference (PCR) is used as a reference signal for the clock recovery system. As is known, the SCR is a time stamp referenced to the encoder clock which recurs in packets of an MPEG-2 program

15 stream at intervals up to 700 ms. The PCR is a corresponding time stamp that recurs in packets of an MPEG-2 transport stream at intervals up to 100 ms. The transport stream is an alternate MPEG-2 bitstream construct which generally provides increased error detection capability relative to the program stream. The SCR and PCR are generally considered to be equivalent time references and, although the discussion

20 following will, for convenience of nomenclature, be based on use of the SCR time stamp, it should be understood that an equivalent clock recovery process would be carried out in the case of the PCR time stamp being provided to the decoder.

With further reference to Figure 1, an SCR time stamp is received at the decoder and provided as an input to Subtractor 10. At the same time, the SCR input

signal is provided as a Load signal to Counter 12, causing the current value of Counter

12, representing the current frequency of the decoder System Time Clock (STC), to be

output therefrom and provided as a second input to Subtractor 10. A difference is

determined by Subtractor 10 between the input SCR value and the current STC value,

5   and an error signal, e, corresponding to that difference is output from Subtractor 10.

After amplification and filtering of that error signal by Low-Pass Filter & Gain 14, the

output thereof, f, is provided as input to Voltage-Controlled Oscillator 16. The output

of the Voltage-Controlled Oscillator 16 is provided to other decoder stages as the

current value of the decoder STC and is also fed back to the input of the clock

10   recovery circuit via Counter 12. Thus, as a new SCR time stamp value arrives at the

input to Subtractor 10, a new error signal will be generated based on the difference

between that new SCR value and the then-current STC value from Counter 12, which

error signal is ultimately translated into a new STC value by Voltage-Controlled

Oscillator 16, thereby maintaining the decoder STC in synchronism with the encoder

15   clock, as represented by the currently received SCR value. (As is well-known, the

standard system clock frequency under the ISO/IEC 13818-1 (MPEG-2) standard is

27 MHz; however, it will be understood that the principle and operation of clock

recovery as described herein is independent of such specific frequency and any other

frequency may also be used).

20   In the second stage of synchronization, the decoder uses the recovered base

clock rate of the encoder along with decoding and presentation time stamps extracted

from fields of the video bitstream to reproduce video frames at exactly the same rate

as that of the transmitter's encoder. Various video format attributes are also extracted

from fields of the video bitstream which provide essential input data to the

synchronization process. For an MPEG-2 compressed video signal, such attributes include the number of pixels per line, the number of lines per frame, and the number of frames per second. And as already noted, these attributes differ as between MPEG-2 video formats, particularly as between standard definition (SD) video and high

5   definition (HD) video, as discussed below.

The MPEG-2 encoding standard contemplates the encoding and transmission of both high definition (HD) video signals and standard definition (SD) video signals. While MPEG-2 permits multiple video formats for both HD and SD, only a single HD encoding format and a single SD format will be discussed herein -- the two formats so

10   discussed representing a preponderance of presently-realized applications of MPEG-2 encoding. As will be apparent to those skilled in the art, however, the principles discussed will be equally applicable to others of the permitted MPEG-2 video formats.

The video formats for MPEG-2 are characterized by a horizontal scanning rate, expressed as a number of pixels per line, a vertical scanning rate, expressed as a

15   number of lines per frame, and a frame rate, expressed as a number of frames per second. A specific HD video format which can be implemented under MPEG-2 is characterized by a horizontal scanning rate of 2200 pixels per line, a vertical scanning rate of 1125 lines per frame, and a frame rate of 30 frames per second, hereafter denoted 30 Hz. [Note that this format is also covered by the Society of Motion Picture

20   and Television Engineers Standard 240M-*Television - Signal Parameters - 1125-Line High-Definition Production Systems* (hereafter SMPTE 240M)] This scanning format, which also constitutes one of the defined picture formats in the Advanced Television Systems Committee Digital Television Standard (hereafter ATSC Standard), can accommodate 1920 active pixels per line and 1080 active lines per frame, in

accordance with the ATSC Standard (and, as well, the SMPTE Standard 274M

Television - 1920 x 1080 Scanning and Interface (hereafter SMPTE 274M)).

The SD video format used herein is characterized by a horizontal scanning rate

of 858 pixels per line, a vertical scanning rate of 525 lines per frame, and a frame rate

5   of 29.97 frames per second, hereafter denoted 29.97 Hz. This scanning format also

constitutes one of the defined picture formats in the ATSC Standard (and is also

defined in the standard: ITU-R BT.601-4, *Encoding parameters of digital television*

for studios), and can accommodate 720 active pixels per line and 480 active lines per

frame.

10   It is noted that, although 30 Hz is the "normal" frame rate for the MPEG-2 HD

and 29.97 Hz is the "normal" frame rate for MPEG-2 SD, the MPEG-2 standard

permits either frame rate to be used with either video format. Note also that the 29.97

Hz frame rate is commonly denoted in the art as "30/1.001," and that convention will

generally be used herein.

15   As is well known, the conversion of an analog video signal to a digital bit

stream is carried out by sampling the analog signal at a sampling rate at least twice the

signal frequency. In the usual case where the sampling rate is selected such that each

digital bit corresponds to one pixel of video information, that sampling rate

corresponds to the total number of pixels processed in a unit of time. Thus, using the

20   video format parameters described above, that sampling rate, which is also

characterized as the pixel clock, will be the product of the horizontal scanning rate,

the vertical scanning rate and the frame rate. In the case of the HD video format, this

pixel clock would be derived as:

$$30 \text{ Hz} \times 1125 \times 2200 = 74.25 \text{ MHz.}$$

Similarly, the pixel clock for the SD video format would be derived as:

$$30/1.001 \text{ Hz} \times 525 \times 858 = 13.5 \text{ MHz}.$$

In the operation of the video decoder, these sampling/scanning frequencies –

i.e. the pixel clock rate, the horizontal scanning rate and the frame rate, must be

5   derived from the decoder STC. For example, considering the case of the HD video

format, extraction of the video format attributes from an MPEG-2 video bit-stream

begins with the derivation of the pixel clock, which is typically derived by

multiplying the recovered 27 MHz base clock by 11 and then dividing by 4. Thus, the

pixel clock rate for this format is derived as: 27 MHz × 11/4 = 74.25 MHz. The

10   horizontal scanning rate for each frame is then derived by dividing the pixel clock by

the total number of pixels per line, which is a constant for a given video format. Thus

a divider is implemented in the decoder having as its dividend the pixel clock rate

(here, 74.25 MHz) and as its divisor the pixels per line for the video format being

decoded (here, 2200). The output of the divider, representing the derived horizontal

15   scanning rate, will be: 74.25 MHz/2200 = 33.75KHz. The frame rate can then be

generated in a second divider by dividing the horizontal frequency by the total number

of scanning lines per frame. For this exemplary HD video format, the decoder frame

rate will be derived as 33.75KHz ÷ 1125 lines/frame = 30 Hz.

Correspondingly for the SD video format case, the pixel clock for the SD

20   video is derived by dividing by 2, the 27 MHz system clock recovered in the first

synchronization stage, to obtain a 13.5MHz pixel clock. The horizontal scanning

frequency can then be derived by dividing this pixel clock by the total number of

pixels per line. For the exemplary SD format described here, the 3.5MHz pixel clock

will be divided by 858 pixels per line to obtain a horizontal scanning frequency of

15.734KHz. The frame rate is then derived by dividing this horizontal scanning

frequency by the total number of scanning lines per frame, here the ATSC standard of

525, to arrive at the current standard frame rate for SD of 29.97 Hz (30/1.001).

Although as set forth above, the standard decoder operations for SD and HD

5   video are arranged to develop frame rates of 30/1.001 and 30 respectively, the ATSC

standard allows for transmission frame rates of 30 and 30/1.001 for all standard

formats. Thus, despite the fact that digital video decoders normally decode an HD

video signal at a frame rate of 30 frames/second, such signal can instead be

transmitted at a 30/1.001 frames/second rate. Similarly, while a decoder normally

10   decodes an SD video signal at a frame rate of 30/1.001 frames/second, the ATSC

standard allows for transmission of such SD signal at 30 frames per second rate. In

such case, the SD and HD signals decoded and reproduced by the decoder will not be

synchronized with the signals transmitted by the encoder. It will be appreciated that

without such synchronization, significant errors in the reconstruction of the digital

15   video signal can occur. For example, it is known that each digital display device

decoder has a bitstream buffer at its input, which is filled for some period of time

before the first picture is removed for decoding. If the decoder rate is faster than the

encoder rate, less than the entire bitstream is decoded from the bitstream buffer by the

digital display device. This is referred to as bitstream buffer underflow. Conversely,

20   if the decoder rate is slower than the encoder rate, then bitstream buffer overflow

occurs. Bitstream buffer underflow is likely to cause the resulting picture to freeze

while an overflow will result in data loss and could have disastrous results.

The need to ensure that a digital video decoder is capable of synchronizing

incoming SD and HD signals encoded and transmitted at a frame rate different from

the decoders normal expectation (based on the video format being processed) is addressed by Applicant's invention through alternate embodiments. In the first embodiment, a clock frequency modification means is incorporated into the decoder function to act on the output of the clock recovery system – *i.e.*, the STC. Since the

5   decoder-derived pixel clock rate, horizontal scanning rate and frame rate are each linear functions of the STC frequency, a modification of the STC frequency proportional to the desired modification of those functions (*i.e.*, the modification needed to provide synchronization at the non-standard frame rate) will ultimately be translated into corrected values for those functions.

10   The frequency modification means of this embodiment is schematically illustrated in Figure 2. As will be seen from the figure, the output of the decoder clock recovery system 20, representing the decoder STC at a nominal 27 MHz frequency, is applied as an input to the frequency modification means 22, which in the illustrated embodiment is constituted as a phase locked loop (PLL). The PLL

15   operates to apply one of three ratios as a multiplier for the input STC, and to thereby produce as an output of the frequency modification means a modified STC as the product of the applied ratio and the input STC. Those ratios correspond to various states of the encoded frame rate (as derived from fields of the input bitstream to the decoder) relative to the decoder's frame-rate expectation for the video format being

20   decoded. Specifically, a first ratio (1/1) corresponds to an identity between the encoded frame rate and the decoder frame-rate expectation; a second ratio (1000/1001) corresponds to an encoded frame rate of 30/1001 Hz and a decoder frame-rate expectation of 30 Hz; and the third ratio (1001/1000) corresponds to an encoded frame rate of 30 Hz and a decoder frame-rate expectation of 30/1,001 Hz.

These ratios and the corresponding frame-rate relationships are set forth in tabular

form in Table 1.

TABLE 1

Encoded Frame Rate	Decoder Frame-Rate Expectation	Ratio Factor
29.97	29.97	1.000
29.97	30.00	.999 (1000/1001)
30.00	29.97	1.001 (1001/1000)
30.00	30.00	1.000

Software, which may be run by the decoder's main processor or by a separate

processor associated with the PLL, is implemented to detect the encoded frame rate in

5   the input bitstream fields and to compare that encoded frame rate with the decoder

frame-rate expectation for the video format being transmitted. After comparing the

encoded frame rate with the decoder frame-rate expectation, the software selects the

appropriate PLL ratio (as illustrated in the table above) and directs the PLL to apply

that ratio to the inputted STC. The output of the PLL will thus be either the STC

10   frequency of 27 MHz, or the modified clock frequencies of 26.973 MHz or 27.027

MHz.

By use of a clock frequency modification arrangement according to the

invention, the video decoder's frame rate can be successfully synchronized with the

frame rate of the encoder for both SD and HD signals, irrespective of the frame rate

15   selected at the encoder. This may be further understood with reference to the

following table wherein the first two rows apply to an HD signal and the latter two

rows to an SD signal

TABLE 2

RATIO FACTOR	BASE CLOCK (MHz)	PIXEL CLOCK (MHz)	PIXELS/ LINE	LINES/ FRAME	FRAME RATE (Hz)
1.000	27.000	74.2500	2200	1125	30.00
1000/1001	26.973	74.1758	2200	1125	29.97
1.000	27.000	13.5000	858	525	29.97
1001/1000	27.027	13.5135	858	525	30.00

Thus it can be seen, for example, that where an SD signal is encoded with a frame rate of 30 Hz, a modifying factor of 1001/1000 (or 1.001) can be applied to the base clock frequency to arrive at a modified base clock frequency of 27.027 MHz.

5   This modified signal will then be provided to the decoder synchronization-rate derivation functions. In this case the modified pixel clock will then be 13.5135 MHz (27.027/2). Dividing this number by the total number of pixels per line (858) and the total number of scanning lines per frame (525) will result in a decoded frame rate of 30 kHz.

10   In an alternative embodiment of the invention, a clock frequency modification arrangement to provide the necessary modification to the STC rate for decoder synchronization (as in the prior embodiment) is realized through an adaptation of the decoder clock-recovery system itself. With this embodiment, a modified STC frequency is produced at the output of the clock recovery system which can be used to

15   derive correct synchronization values in the case of a non-standard encoder frame rate. The methodology of this embodiment will be better understood by reference to Figure 3, which depicts a clock recovery system substantially corresponding to that of Figure 1 with the addition of a Multiplier unit 38 inserted to receive the System Time Clock output from Counter 32, and providing an output thereof to Differentiator and

Subtractor 30, which replaces Subtractor 10 of the standard clock-recovery system of

Figure 1. In the operation of this embodiment, the SCR signal is provided to a

Differentiator and Subtractor device 31 and, as well, to Counter 32 as a Clear signal.

[As with the discussion of Figure 1 above, because of the substantial equivalence

5   between the PCR and SCR time stamps, the discussion here is framed in terms of only

the SCR; it should be understood however, that this embodiment will operate equally

well with the PCR reference.] The Counter 32 is cleared after it receives each SCR or

PCR, and thus, the value of the Counter 32 is the number of clock ticks between the

arrival of two SCR's or two PCR's. An output of the Counter 32 is then fed into the

10   input of Multiplier 38, the output of which is, in turn, provided as an input to

Differentiator and Subtractor 30. The Differentiator evaluates the difference between a

received SCR value and the immediately preceding SCR value, as well as the

difference between the Counter output and the Counter value corresponding to that

immediately preceding SCR value. The Subtractor determines a difference between

15   the Differentiator SCR and Counter differences and provides this difference output to

Low-Pass Filter 34. The output of the Low-Pass Filter 34 is then provided to a

Voltage-Controlled Oscillator (VCO) 36, which is preferably a voltage-controlled

crystal oscillator. The modified system clock frequency is then output from VCO 36,

where it is provided as an output to other decoder functions, including

20   synchronization-rate derivation functions, such as are depicted in Figure 2 of the

contemporaneously filed and cross-referenced application S/N _____, and is

also fed back to Counter 32.

       In the operation of Multiplier 38, the System Time Clock output of Counter 32

will constitute the multiplicand, and the multiplier will be selected from one of three

ratios corresponding to various states of the encoded frame rate relative to the decoder's frame-rate expectation for the video format being decoded. Specifically, a first ratio (1/1) corresponds to an identity between the encoded frame rate and the decoder frame-rate expectation; a second ratio (1001/1000) corresponds to an encoded

5 frame rate of 30/1001 Hz and a decoder frame-rate expectation of 30 Hz; and the third ratio (1000/1001) corresponds to an encoded frame rate of 30 Hz and a decoder frame-rate expectation of 30/1,001 Hz.

Software, which may be run by the decoder's main processor or by a separate processor associated with the Multiplier, is implemented to detect the encoded frame

10 rate in the input bitstream fields and to compare that encoded frame rate with the decoder frame-rate expectation for the video format being transmitted. Based on that information, the software selects the appropriate Multiplier ratio and causes the Multiplier to apply that ratio to the multiplicand input. The development of appropriate software to carry out these functions will be well within the skill of those

15 in the art.

In the operation of the method of this embodiment, upon setting the Multiplier 38 input to 1.000, the modified system clock frequency output from the VXO 36 is a nominal 27 MHz. In a similar manner, when the Multiplier 38 input is set to 1000/1001, the modified system clock frequency is 27.027 MHz, and when it is set to

20 1001/1000, the modified system clock frequency is 26.973 MHz.

While details of the invention are discussed herein with reference to particular examples to which the principles of the present invention can be applied, the applicability of the invention to other devices and equivalent components thereof will become readily apparent to those of skill in the art.

Accordingly, it is intended that all such alternatives, modifications, permutations, and variations to the exemplary embodiments can be made without departing from the scope and spirit of the present invention.